Schematic and Layout Guidelines for High-Speed Data Converters

This technical discussion presents proper layout techniques, component selection, and placement for high-speed analog-to-digital converters (ADCs) commonly used in IF and baseband applications. It uses the high-resolution, high-speed data-converter family, MAX12553, MAX12554, and MAX12555, as an example of guidelines that help establish an optimized schematic, proper high-speed layout techniques, bypassing and decoupling tips, thermal management guidelines, as well as component selection and placement.

Introduction

This paper provides a concise resource for schematic and layout suggestions for high-speed data converters. It supplements the schematic and PC-board layout information provided in the component and evaluation-board kit data sheets. The user should consider his specific application and review all these available resources to optimize device performance in the intended application. Maxim's 14-bit analog-to-digital (ADC) converters, the MAX12553, MAX12554, and MAX12555, are used as examples. These parts are optimized for sampling rates of 65Msps/80Msps/95Msps, respectively, and target all IF and baseband applications.

This paper is broken into three sections, General Suggestions, Schematic Suggestions, and Layout Suggestions. The General Suggestions section gives an overview of the design practices that will provide the best overall device performance in the application. It discusses best practices in general terms of external component placement around the device. Suggestions regarding the physical PC-board itself are presented. The Schematic Suggestions section provides recommended component values for the most critical and sensitive device pins. The Layout Suggestions section, finally, details component placement recommendations around the device, identifies which external components should be placed on the top layer or bottom layer. Additional information regarding the PC board is provided.

Please refer to
Figure 1 for an illustration of the pinout and **Table 1** for the pin description for this family of ADCs. The evaluation (EV) kit includes multiple options that allow for single-ended or differential clock, single-ended or differential clock analog input, internal/external reference, etc. Therefore, the EV kit schematics (**Figure 2** and **Figure 3**) accommodate many more external components and configurations than would be used in a normal application. **Figure 4** and **Figure 5**, finally, provide the silkscreen and component placement for the top and the bottom layer of the EV kit.

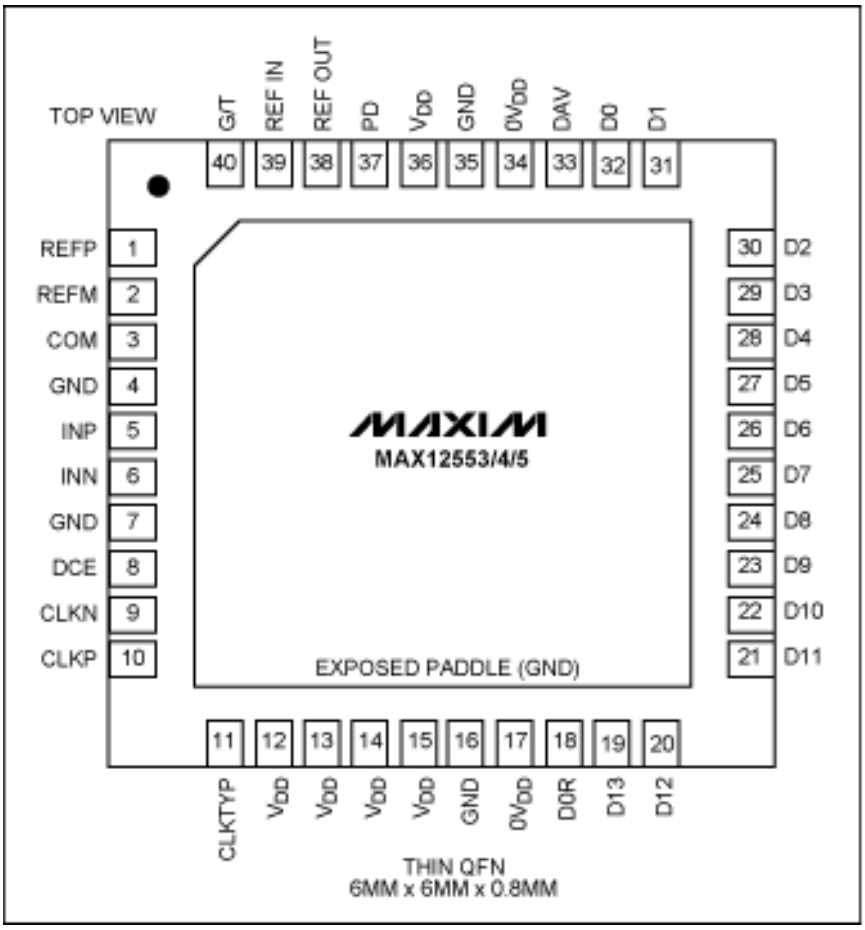


Figure 1. MAX12553, MAX12554, and MAX12555 Pinout

Table 1. Pin Description

PIN	NAME	FUNCTION
1	REFP	Positive Reference I/O. The full-scale analog input range is ±(V_{REFP}-V_{REFN}) x 2/3. Bypass REFP to GND with a 0.1µF capacitor. Connect a 1µF capacitor in parallel with a 10µF capacitor between REFP and REFN. Place the 1µF REFP to REFN capacitor as close to the device as possible on the same side of the PC board.
2	REFN	Negative Reference I/O. The full-scale analog input range is ±(V_{REFP}-V_{REFN}) x 2/3. Bypass REFN to GND with a 0.1µF capacitor. Connect a 1µF capacitor in parallel with a 10µF capacitor between REFP and REFN. Place the 1µF REFP to REFN capacitor as close to the device as possible on the same side of the PC Board.
3	COM	Common-Mode Voltage I/O. Bypass COM to GND with a 2.2µF capacitor. Place the 2.2µF COM to GND capacitor as close to the device as possible. This 2.2µF capacitor can be placed on the opposite side of the PCB and connected to the MAX12553 through a via.
4, 7, 16, 35	GND	Ground. Connect all ground pins and EP together.
5	INP	Positive Analog Input.

6	INN	Negative Analog Input.
8	DCE	Duty-Cycle Equalizer Input. Connect DCE low (GND) to disable the internal duty-cycle equalizer. Connect DCE high (OV_{DD} or V_{DD}) to enable the internal duty-cycle equalizer.
9	CLKN	Negative Clock Input. In differential clock input mode (CLKTYP = OV_{DD} or V_{DD}), connect the differential clock signal between CLKP and CLKN. In single-ended clock mode (CLKTYP = GND), apply the single-ended clock signal to CLKP and connect CLKN to GND.
10	CLKP	Positive Clock Input. In differential clock input mode (CLKTYP = OV_{DD} or V_{DD}), connect the differential clock signal between CLKP and CLKN. In single-ended clock mode (CLKTYP = GND), apply the single-ended clock signal to CLKP and connect CLKN to GND.
11	CLKTYP	Clock Type Definition Input. Connect CLKTYP to GND to define the single-ended clock input. Connect CLKTYP to OV_{DD} or V_{DD} to define the differential clock input.
12-15, 36	V_{DD}	Analog Power Input. Connect V_{DD} to a 3.15V to 3.60V power supply. Bypass V_{DD} to GND with a parallel capacitor combination of $\geq$2.2µF and 0.1µF. Connect all V_{DD} pins to the same potential.
17, 34	OV_{DD}	Output-Driver Power Input. Connect OV_{DD} to a 1.7V to V_{DD} power supply. Bypass OV_{DD} to GND with a parallel capacitor combination of $\geq$2.2µF and 0.1µF.
18	DOR	Data Out-of-Range Indicator. The DOR digital output indicates when the analog input voltage is out of range. When DOR is high, the analog input is beyond its full-scale range. When DOR is low, the analog input is within its full-scale range.
19	D13	CMOS Digital Output, Bit 13 (MSB)
20	D12	CMOS Digital Output, Bit 12
21	D11	CMOS Digital Output, Bit 11
22	D10	CMOS Digital Output, Bit 10
23	D9	CMOS Digital Output, Bit 9
24	D8	CMOS Digital Output, Bit 8
25	D7	CMOS Digital Output, Bit 7
26	D6	CMOS Digital Output, Bit 6
27	D5	CMOS Digital Output, Bit 5
28	D4	CMOS Digital Output, Bit 4
29	D3	CMOS Digital Output, Bit 3
30	D2	CMOS Digital Output, Bit 2
31	D1	CMOS Digital Output, Bit 1

32	D0	CMOS Digital Output, Bit 0 (LSB)
33	DAV	Data-Valid Output. DAV is a single-ended version of the input clock that is compensated to correct for any input clock duty-cycle variations. DAV is typically used to latch the MAX12553 output data into an external back-end digital circuit.
37	PD	Power-Down Input. Force PD high for power-down mode. Force PD low for normal operation.
38	REFOUT	Internal Reference Voltage Output. For internal reference operation, connect REFOUT directly to REFIN or use a resistive divider from REFOUT to set the voltage at REFIN. Bypass REFOUT to GND with a ≥0.1µF capacitor.
39	REFIN	Reference Input. In internal reference mode and buffered external reference mode, bypass REFIN to GND with a ≥0.1µF capacitor. In these modes V_{REFP} - V_{REFN} = VREFIN x 3/4. For unbuffered external reference-mode operation, connect REFIN to GND.
40	G/ /T\	Output Format Select Input. Connect G/ /T\ to GND for the Two's complement digital output format. Connect G/ /T\ to OV_{DD} or V_{DD} for the Gray code digital-output format.
-	EP	Exposed Paddle. The MAX12553 relies on the exposed paddle connection for a low-inductance ground connection. Connect EP to GND to achieve specified performance. Use multiple vias to connect the top-side PCB ground plane to the bottom-side PCB ground plane.

General Suggestions

- In general, multilayer boards with solid ground planes and power planes produce the highest level of signal integrity.
- The MAX12553, MAX12554, and MAX12555 requires high-speed board-layout design techniques, including a solid ground-plane connection to the exposed paddle.
- Keep the inner layer ground-plane integrity on the analog side of the MAX12553, MAX12554, and MAX12555 totally solid, with absolute minimum voids. Stagger vias, use very small via clearances, etc., to minimize voids. Also, keep a solid ground beneath the critical components, especially the REF capacitors on pins 1 and 2, the pin 3 COM bypass, and the small valued capacitors around the analog input pins 5 and 6.
- Confine the different input and output signals to well-defined layer allocations, all analog inputs in layer X, all digital output on layer Y, all clocks on layer Z, etc. Then try to trap each layer between two solid ground planes or as microstrip.
- Use power-supply planes as opposed to ground traces to minimize inductance for these signals and to minimize overall noise. If power traces are used, they should be made physically wide to minimize IR drop and inductance.
- For GND and V_{DD} (power connections), we recommend multiple 18mil drill size vias.
- All MAX12553, MAX12554, and MAX12555 GNDs and the exposed paddle (EP) must be connected to the same ground plane. The MAX12553, MAX12554, and MAX12555 relies on the EP connection for a low-inductance ground connection using multiple vias to the designated ground layer. The number of vias required depends on the hole size. As a

guideline, Maxim uses a matrix of 5 x 5 (25 total) 13 mil vias. A minimum of 12 vias is required.

- The most critical connections in and out of the MAX12553, MAX12554, and MAX12555 are considered analog input, reference pins, clock, and the digital output traces. The most critical pins are 1, 2, 3, 5, 6, 9, 10, 38, and 39.
- Traces connecting bypass and critical capacitors around the ADC should be as wide as possible to minimize resistance and inductance. Trace widths greater than or equal to 10mils are recommended. Ground traces should be made as wide as possible if the component is not located directly on the ground plane. This includes any ground thermals used in PCB designs.
- If thermals are used to route a bypass capacitor to GND, use two thermals per capacitor with a via at the GND end of each thermal to minimize inductance.
- Route high-speed digital signal traces away from the sensitive analog traces, clock traces, and REFP (pin 1) and REFN (pin 2).
- Keep all signal lines (including REFP and REFN) short and free of 90° turns.
- Ensure that the differential-analog-input network layout is symmetrical and that all parasitics are balanced equally.
- Locate all bypass capacitors as close to the device as possible, preferably on the same side of the PCB as the ADC, using surface-mount devices to limit the inductance (described in greater detail in the *Layout Suggestions* section below).
- In general all GND bypass vias should have a drill size of 18mils.
- This device requires separate analog and digital power supplies for best performance.
- The MAX12553, MAX12554, and MAX12555 allows for either differential or single-ended signals to the clock inputs.
- The MAX12553, MAX12554, and MAX12555 accepts differential or single-ended analog input signals. Differential signals provide optimum performance.
- The device EP acts as the main ground for the device and therefore must be properly attached to the designated ground plane.
- Use ground 'island' between the ADC circuit and any other adjacent circuitry that might be included on the board. If, for example, multiples ADCs are used on a single board, separate their associated circuits with ground plane between them.

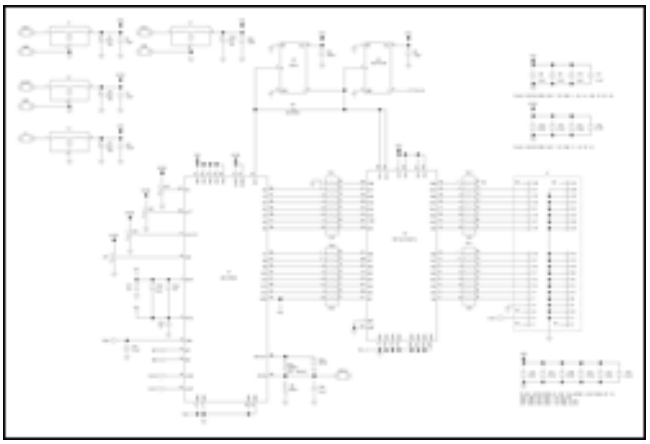
Schematic Suggestions

(Refer to Figure 2 and Figure 3)

- (Pin 1, REFP): Bypass REFP to GND with a high-frequency (up to 1.0uF) ceramic capacitor on the top side of the board. Keep all REFP traces short.
- (Pin 2, REFN): Bypass REFN to GND with a high-frequency (up to 1.0uF) ceramic capacitor on the top side of the board. Keep all REFN traces short.
- (Pin 1, REFP and pin 2, REFN): Include a high-frequency 1uF ceramic capacitor in parallel with a high-frequency 10uF ceramic capacitor between REFP and REFN. Any capacitors connected to pins 1 and 2 must be of good high-frequency quality.
- (Pin 3, COM): Bypass COM to GND with a good high-frequency 2.2uF ceramic capacitor.
- (Pins 5 & 6, INP & INN): To achieve best overall AC performance, shunt capacitors should be included on these pins to ground having a value ranging from 5.6pf to 12pf, depending on the application. These capacitor values can be included in the resonant circuit of any anti-aliasing

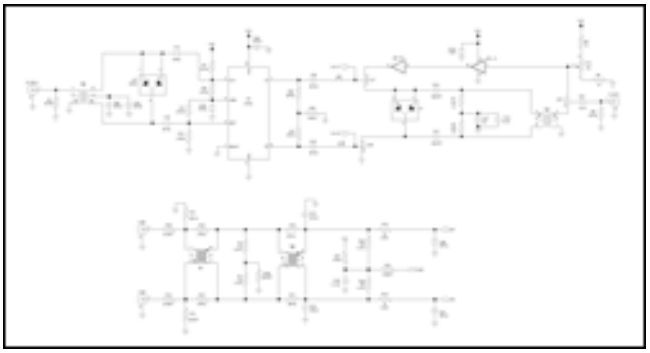
filter driving the ADC and should be located on the top of the board.

- (Pins 12-15, 36, V_{DD}): Bypass V_{DD} to GND with a good high-frequency 0.1uF ceramic capacitor in parallel with a good high-frequency = 2.2uF ceramic capacitor.
- (Pins 17, 34, OV_{DD}): Bypass OV_{DD} to GND with a good high-frequency 0.1uF ceramic capacitor in parallel with a good high-frequency $\geq$ 2.2uf ceramic capacitor.
- (Pins 19-32, D13 - D0): Include series resistors from the data output pins to their respective load. These resistors limit the high-frequency edge current into the internal chip GND from the output logic drivers. Choose a value, when combined with the load capacitance, that will yield an RC time constant of approximately 1ns. Maxim uses a very small and inexpensive resistor array, basically multiple 0402 resistors made in one continuous block. From our EV Kit, reference Panasonic part # EXB-2HV-221J.
- (Pin 38, REFOUT): For internal reference operation, connect REFOUT directly to REFIN or use a resistive divider from REFOUT to set the voltage at REFIN. Bypass REFOUT to GND with a good high-frequency $\geq$ 0.1uF ceramic capacitor.
- (Pin 39, REFIN): In the internal reference mode and buffered external reference mode, bypass REFIN to GND with a good high-frequency $\geq$ 0.1uF ceramic capacitor. For unbuffered external reference-mode operation, connect REFIN to GND.



For Larger Image

Figure 2. EV Kit Device Schematic



For Larger Image

Figure 3. EV Kit Analog-Section Schematic

Layout Suggestions

(Refer to Figure 4 and Figure 5)

- Place the MAX12553, MAX12554, and MAX12555 on the top side of the PC board.
- Next, place the 1uF capacitor between pins 1 and 2. This capacitor should be located on the top side of the board as close to these pins as possible. The 1uF capacitor across REFP and REFN (pins 1 and 2) should be as close to the DUT as manufacturing tolerances allow.
- Next, place the bypass capacitors from pin 1 to ground and from pin 2 to ground. These capacitors should be placed next to the shared 1uF capacitor as close as possible, and vias should be used to connect the GND end of these capacitors to the designated analog ground layer (also connected to the device EP). IF there is a ground plane on layer two, this plane should extend under these three to reduce the inductance to pins 1 and 2. For the REFP and REFN ground vias, Maxim uses a drill diameter of 18mils, which has been oversized by 3mils to account for plating. The final hole size should approximate15mils.
- Next, place the 10uF capacitor between pins 1 and 2. If sufficient space is not available on the top layer for this capacitor, it can be included on the bottom of the board using vias to route the signals, as is done on the EV kit. Minimize the overall trace lengths connecting this capacitor to the device pins.
- The trace lengths to and from pins 1 and 2 should be short in length and should be matched. Restated, they should be symmetrical and the same length.
- Next, place the 2.2uF capacitor from pin 3 to GND as close as possible to the device. This capacitor can be located on the bottom of the board and connected to pin 3 using a 13 mil via if needed. The trace should be kept short.
- All GND pins (pins 4, 7, 16, and 35) should be physically routed to the copper beneath the MAX12553, MAX12554, and MAX12555 using traces.
- It is imperative that the MAX12553, MAX12554, and MAX12555 EP be properly connected to the designated ground plane (preferably layer 2). This can only be accomplished using a sufficient number of vias to minimize inductance–with the number dependent on the hole size. As a guideline, Maxim recommends a matrix of 5 x 5 (25 total) 13mil vias be used; a minimum of 12 mils is required.
- The analog input circuit should be balanced. This means that the trace lengths from the driving source (amplifier, filter, etc.) to the differential inputs should be the same length, and the placement of the components should be symmetrical to one another so that all parasitics are balanced equally. These lines should be kept short to minimize inductance and pick-up.
- Minimize the shunt-capacitor trace lengths on the analog input pins 5 and 6 by placing them close to the device pins on the top of the board.
- A single layer (preferably layer 2) should be used as solid analog ground to which the MAX12553, MAX12554, and MAX12555 EP is connected using the recommended via array.
- Clock suggestions (pins 9 and 10):
  The clock inputs are as sensitive as the analog inputs and reference pins. Treat the clock lines the same as you would the analog signal lines. Avoid running the clock lines close to any digital output signals. If multiple ADCs are used on the board, separate clock line pairs to minimize noise and signal pick-up from the other ADC section. Clock signals should not be on the same layer as the data output lines. If they are, strive to eliminate any coupling that might occur by keeping a relatively large physical distance between the two signal types and by routing GND between the two signal types.

  For a differential clock input, we recommend a typical value of 1.4VP-P because that is used to characterize these devices. It is not, however, the peak-to-peak input clock-signal swing

that is most important, but rather the slew rate to yield fast rise and fall times. Also, an internal differential amplifier provides gain and further squares-up the signal. On the EV kit, we step-up the clock input using a center-tapped transformer to ensure fast rise and fall times, and then limit the amplitude to 1.4VP-P using diodes. For a single-ended clock, the edges should be sharp, with the max and min voltages specified in the data sheet as $0.8V_{DD}$ min for the high logic level and $0.2V_{DD}$ max for the low logic level. The clock common-mode voltage ($1/2V_{DD}$) is provided internally. Recommended interface circuit/driver logic: any of the logic families including input CMOS, LVPECL, LVDS can be used for driving the clock input. For the most demanding applications with high-frequency input signals, very high-speed LVPECL clock distribution is recommended, such as the MAX9320 PECL buffer.

- (Pins 12-15, 36, V_{DD}): best practice is to locate the 0.1uF bypass capacitor right next to the device pins.
- (Pins 17, 34, OV_{DD}): best practice is to locate the 0.1uF bypass capacitor right next to the device pins.
- Data lines (pins 19 to 32): For the output data pins, try to keep the traces from the ADC to the buffer or load IC short. Place the series resistors very close to the ADC and target a total load capacitance of = 10pF to ensure optimal performance. It is very important that the buffer or load IC has a solid ground plane back to the MAX12553, MAX12554, and MAX12555 EP ground to achieve optimum AC performance. If the data lines are routed on the top or bottom layer (microstrip technique), the adjacent layer must be a ground plane to form effective transmission lines. If the data lines are routed on an inner layer (stripline technique), both adjacent layers must be at ground potential to form an effective transmission line. Confine the digital-signal outputs to be tightly arranged in a single bus to control the return current path. Also, minimize the ground plane voids (created by digital-signal vias) between the MAX12553, MAX12554, and MAX12555 and digital load, perhaps through staggering the via arrangement when the data lines are dropped to an inner layer.
- Bypass capacitors to REFOUT and REFIN (pins 38 and 39) must be located close to the device pins using short traces and grounded directly to the device ground plane.

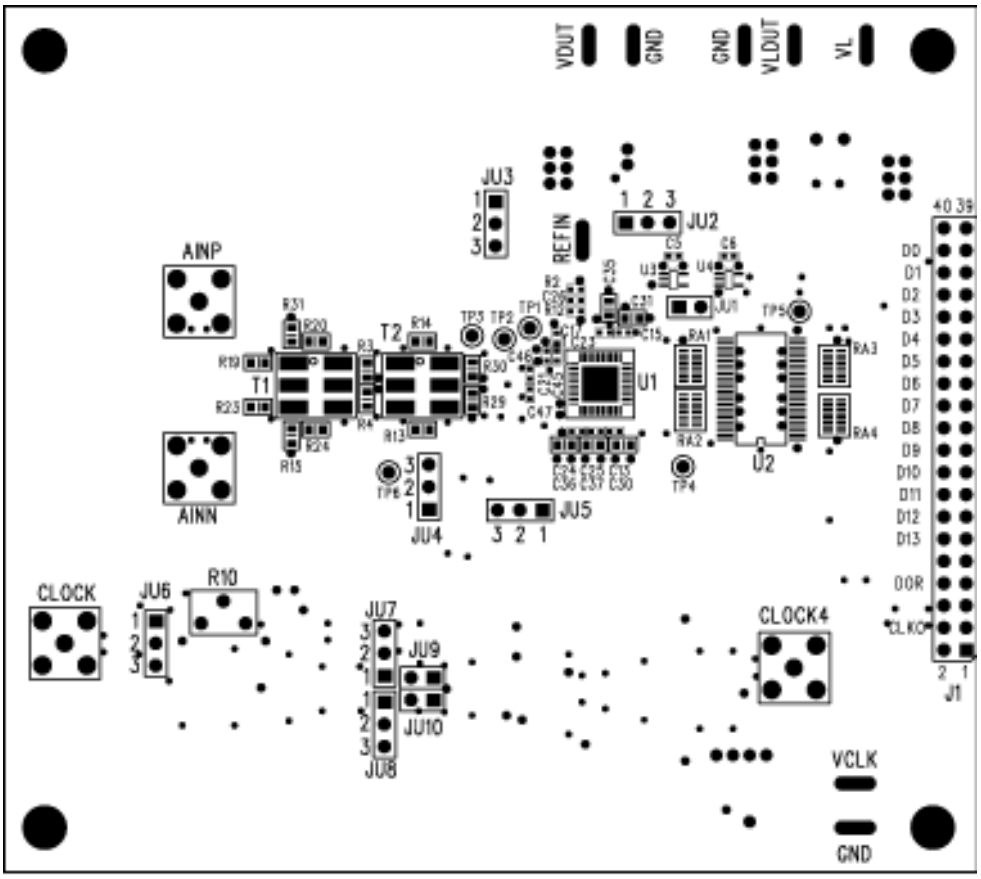


Figure 4. EV Kit Top-Side Silkscreen and Component Placement

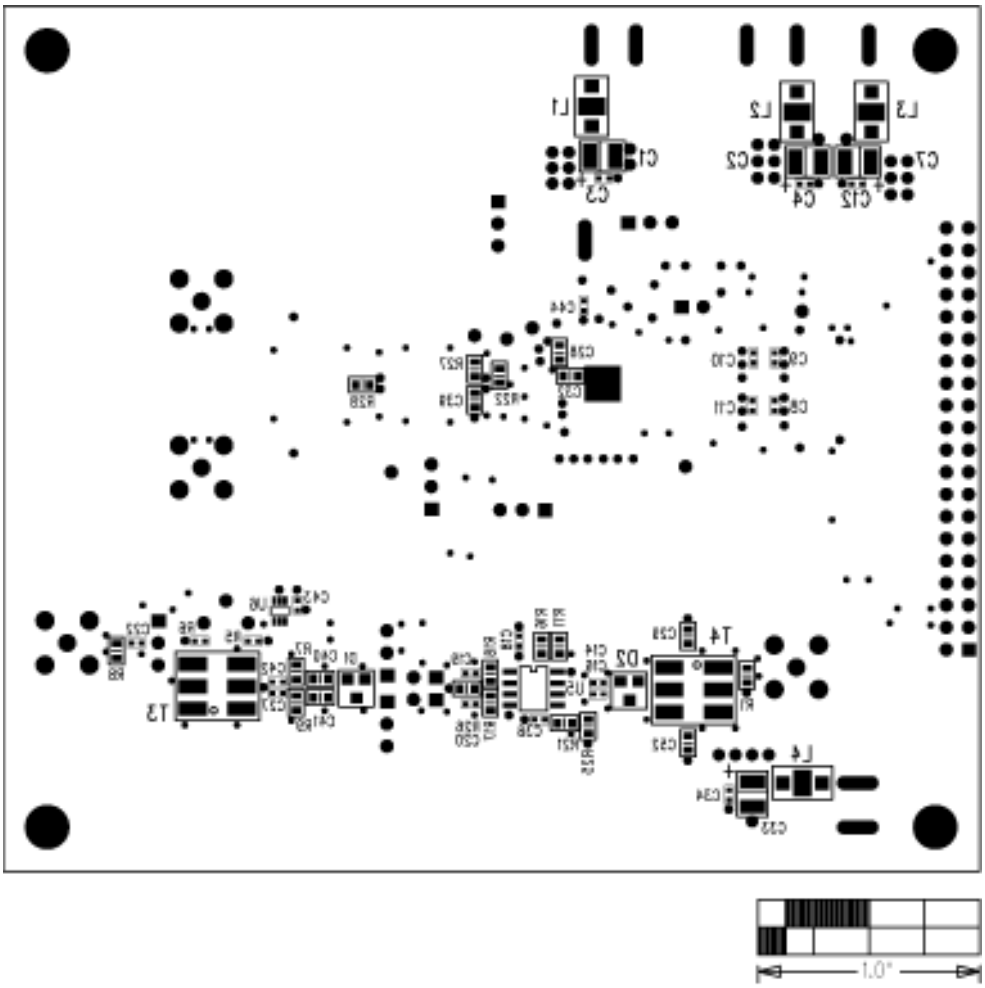


Figure 5. EV Kit Bottom-Side Silkscreen and Component Placement

Conclusion

If the user follows the suggestions provided in this application note to supplement information in the device and EV-kit data sheets, device performance will be optimized in the intended application.

More Information

MAX12553: QuickView -- Full (PDF) Data Sheet -- Free Samples

MAX12554: QuickView -- Full (PDF) Data Sheet -- Free Samples

MAX12555: QuickView -- Full (PDF) Data Sheet -- Free Samples

MAX9320: QuickView -- Full (PDF) Data Sheet -- Free Samples